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10/611,400

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS: Mats Lindstrom et al.	DOCKET NO.: CX03001USU(02CXT0077D)
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	CUSTOMER NO. 34408

TITLE: SATELLITE TRANSCODER

Certificate of Transmission
I hereby certify that this correspondence (along with any paper referred to as being attached or enclosed) is being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (571) 273-8300, on July 31, 2007.

Jeffrey C. Wilk

July 31, 2007

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

DECLARATION UNDER 37 CFR § 1.131

MATS LINDSTROM declares that he is one of three joint inventors who on June 30, 2003, filed the above-referenced application;

That the invention was conceived in this country long prior to February 13, 2003 (the "Effective Date"), the filing date of U.S. Provisional Application No. 60/447,112, to which U. S. Non-Provisional Patent Application 10/736,434, entitled "Communications Signal Transcoder," filed December 15, 2003, claims priority;

That long prior to the Effective Date, he and the other joint inventors prepared a description and drawings of their invention in a document entitled "QPSK Transcoder System Architecture V 1.0," a true and correct copy of which is attached hereto as Exhibit A;

That subsequently the inventors' employer, Conexant Systems, Inc., elected to file a patent application claiming the inventions described in said document and on or about April 2, 2003, contacted The Eclipse Group to commence preparation of the patent application; and

That thereafter drafts of the patent application were prepared and reviewed by the inventors, and the patent application was filed on June 30, 2003.

The undersigned Declarant further states that the above statements were made with the knowledge that willful false statements and the like are punishable by fine and/or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that any such willful false statement may jeopardize the validity of the above-referenced application or any patent resulting therefrom.

Dated: July 31, 2007

Respectfully submitted,

MATS LINDSTROM
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QPSK Transcoder System Architecture V 1.0

Name: Chi-ping Nee

Date: Jan. 30, 2001

EXHIBIT A

Revision History

Version	Released Date	Update
1.0	01/30/2003	Initial Release.

Table of Content

1. Overview

EchoStar is considering a backward-compatible solution for the deployment of their new 8PSK/Advanced QSPK modulation scheme. The solution consists of a QPSK Trancoder that can converts 8PSK/Advanced QSPK into DVB QPSK signals. This memo summarizes the ongoing discussion of system architecture among: (In alphabetical order)

Avi Krieger, Chi-ping Nee, Efi Dalumi, Eran Arad, Gadi Kalit, Mats Lindstrom, John Roberson, Ramaswamy Murali, Shimon Gur, Yoav Goldenberg, Yoav Hebron

As shown in Figure 1, the Transcoder (new Set-top box) will comprise of:

1. 8PSK/Advanced QPSK Demodulator (Mustang): This includes tuner, base-band demodulator and FEC decoder. The base-band demodulator and decoder are defined in Mustang project, which is beyond the scope of this report. The output of Mustang is a MPEG transport stream that contains multiple programs.
2. MPEG Remux: Some old set-top boxes in the field have fixed symbol rate, e.g. 20Msps. Since Mustang can deliver in general higher data rate, discarding some programs in the MPEG transport stream is necessary. MPEG Remux will unpack MPEG Transport Stream, filter out unwanted program, and generate a new MPEG Transport Stream. It should output another MPEG transport stream whose data rate ultimately matches the output QPSK symbol rate.
3. QPSK Encoder/ Modulator: This unit encodes the output of MPEG Remux and modulates into an output digitized base-band signal per DVB spec. The operating include Reed-Solomon encoding, interleaving, convolutional encoding, and base-band pules shaping.
4. Up-converter: convert base-band signal to analog RF signal. A separate report prepared by RF group will have more details on this.
5. 13V/17V Slave device: This unit can demodulate and decode EchoStar Legacy mode protocol from old set-top box. Currently, Camaric has implemented the master device of EchoStar Legacy mode.
6. Micro-controller: It will interpret the received message from 13V/18V Slave device and perform channel change operation. It may also perform other non real-time tasks such as acquisition state machine.
7. Memory: There may be some flash memory needed to store software. Software needs to optimize the footprint

Questions to Marketing:

1. *Is QPSK Encoder/Modulator only per DVB? Is DSS and DCII not needed? The rest of this report will assume DVB only.*
2. *Does EchoStar ever consider any communication between old and new set-top box other than 13V/18V? How about DiSEqC? The rest of this report will assume 13V/17V mode only.*
3. *Is the output carrier frequency of Up-converter fixed or adjustable? Mats suggests a fixed 974MHz to simplify the design.*

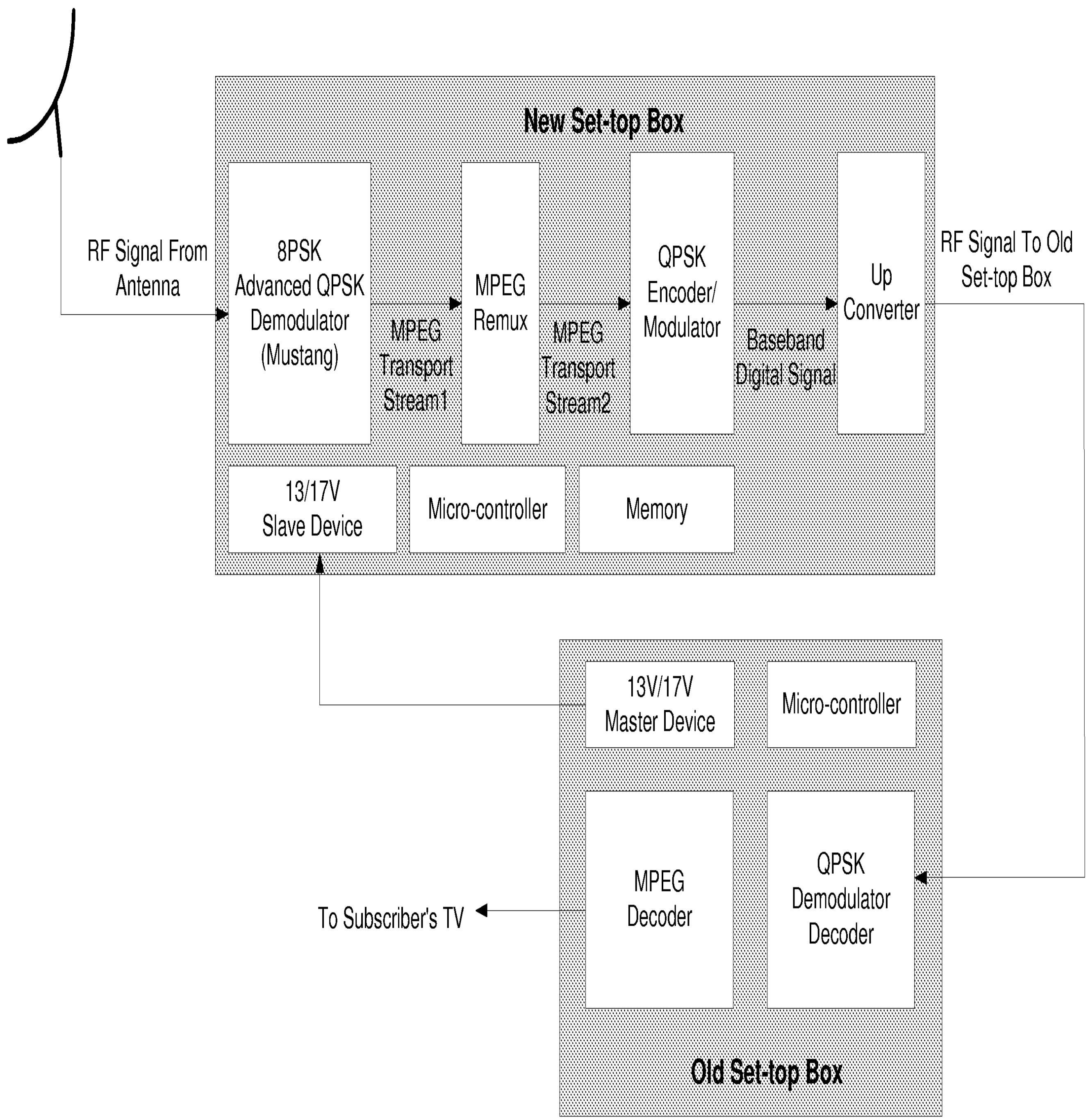

Figure 1: Overview of Trancoder and old set-top box.

2. MPEG Remux

As shown in Figure 2, MPEG Remux consists of the following units:

1. PID Filtering: Select the desired Program ID (PID) and discard the unwanted package.
2. Rate Matching: Insert Null Package to match the output transport stream with data rate.
3. PCR Re-stamping: Recover system clock (27MHz) and re-stamp Program Clock Reference (PCR) for output transport stream.

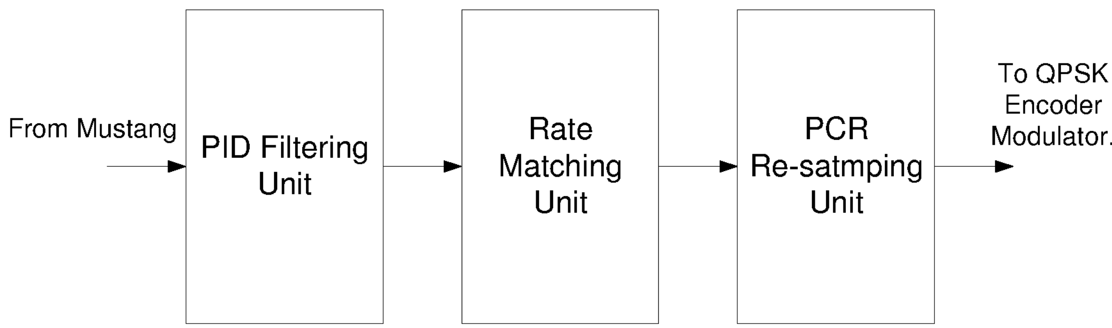

Figure 2: Block Diagram of MPEG Remux.

2.1 PID Filtering Unit

There is a 13-bit PID field in the every MPEG Transport Stream package header. PID Filtering Unit maintains a table with a list of PID interested. Whenever an MPEG transport stream package is received, it compares the PID with the table and decides whether to keep it or discards it.

According to John Roberson, as many as 32 PID is sufficient. Since a transport stream may carry multiple program as well as private data, outputting one broadcast is not equivalent to keeping only one PID.

Question to Marketing:

Need to ask EchoStar the maximal number of PIDs required for QPSK Transcoder.

In the rest of memo, we will assume 32 desired PIDs can be stored in the table. The possible hardware architecture of PID Filtering Unit is illustrated in Figure 2.1. Since PID is always located at 12th to 25th bits of a MPEG transport stream package, a simple state machine should be able to retrieve PID. Suppose one comparison is made at every bit clock cycle. At most 57-bit FIFO is needed to buffer the package, in additional to 13 bit PID FIFO.

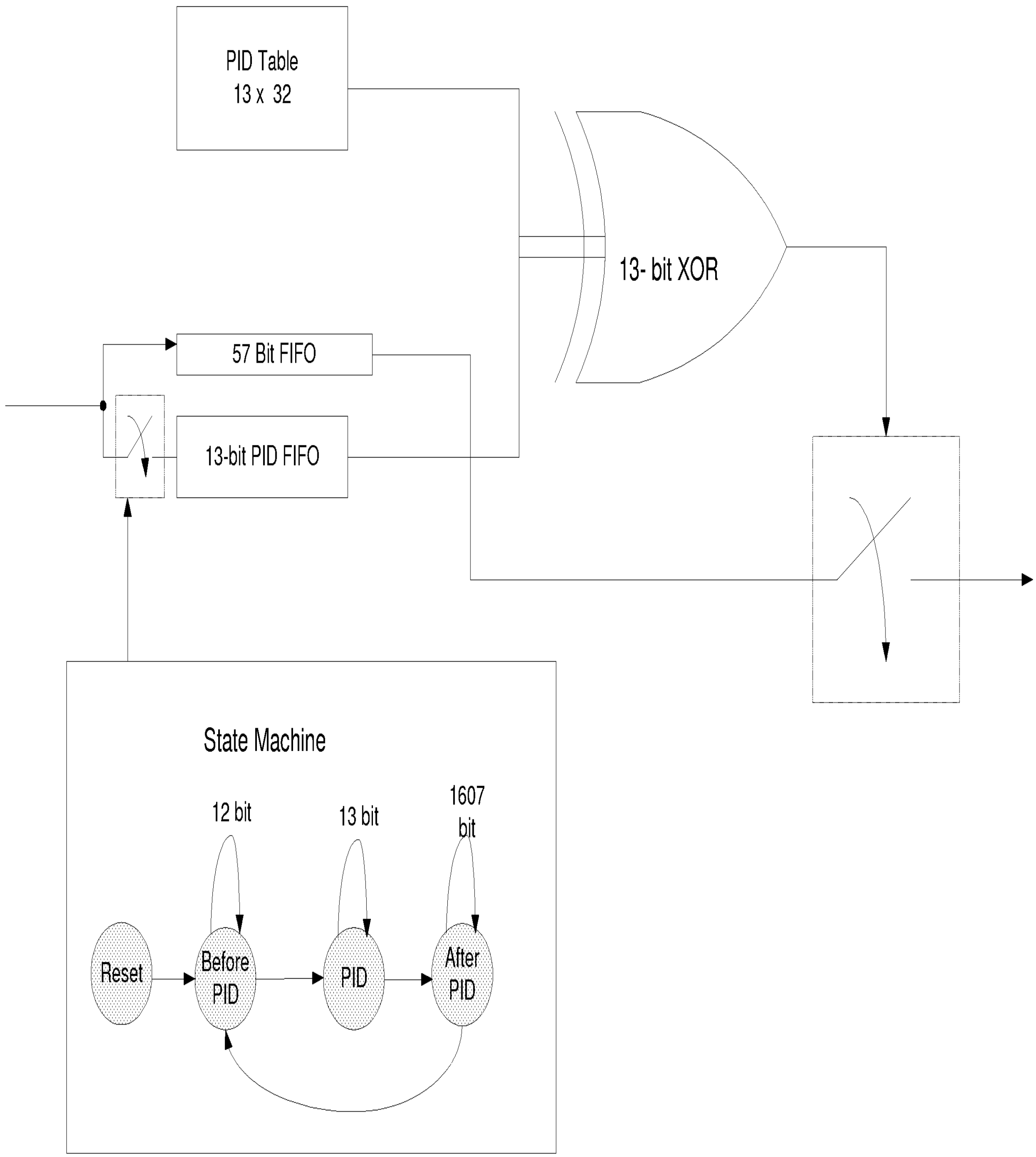

Figure 2.1: Possible implementation of PID Filtering Unit.

2.2 Rate Matching Unit

Rate Matching Unit occasionally inserts null package such that the final output data rate can match the request symbol rate according to the following equation:

(Output MPEG Transport Stream Data Rate) = 2 x (Request Symbol Rate) x (Viterbi Code Rate)

Since the output of PID Filtering Output can be jittery, it is necessary to buffer the output. The size of the buffer depends on how jittery the desired PID is distributed in MPEG transport stream. Fortunately, there is a 2244-byte (11 RS codewords) interleaver memory in QPSK Encoder/Modulator. This memory may be sufficient to smooth the jitter.

Action Item

Compute the maximal tolerable jitter per 11 RS codewords. Marketing also need to find out the requirement.

Suppose Interleaver's memory is sufficient for buffering. Rate Matching Unit can be designed as illustrated in Figure 2.2. A Null Package Insertion circuitry can use

1. The Convolutional Encoder input clock from QPSK Encoder / Modulator; and
2. The FIFO depth of Interleaver buffer.

A loop filter is necessary to determine whether a Null Package should be inserted. This design is very similar to clock smoothing design in Camaric. The insertion of null package can be very simple. It uses the time gap when a package is discarded to insert the null package. Therefore, loop filter need some signal from PID Filtering Unit to utilize this gap.

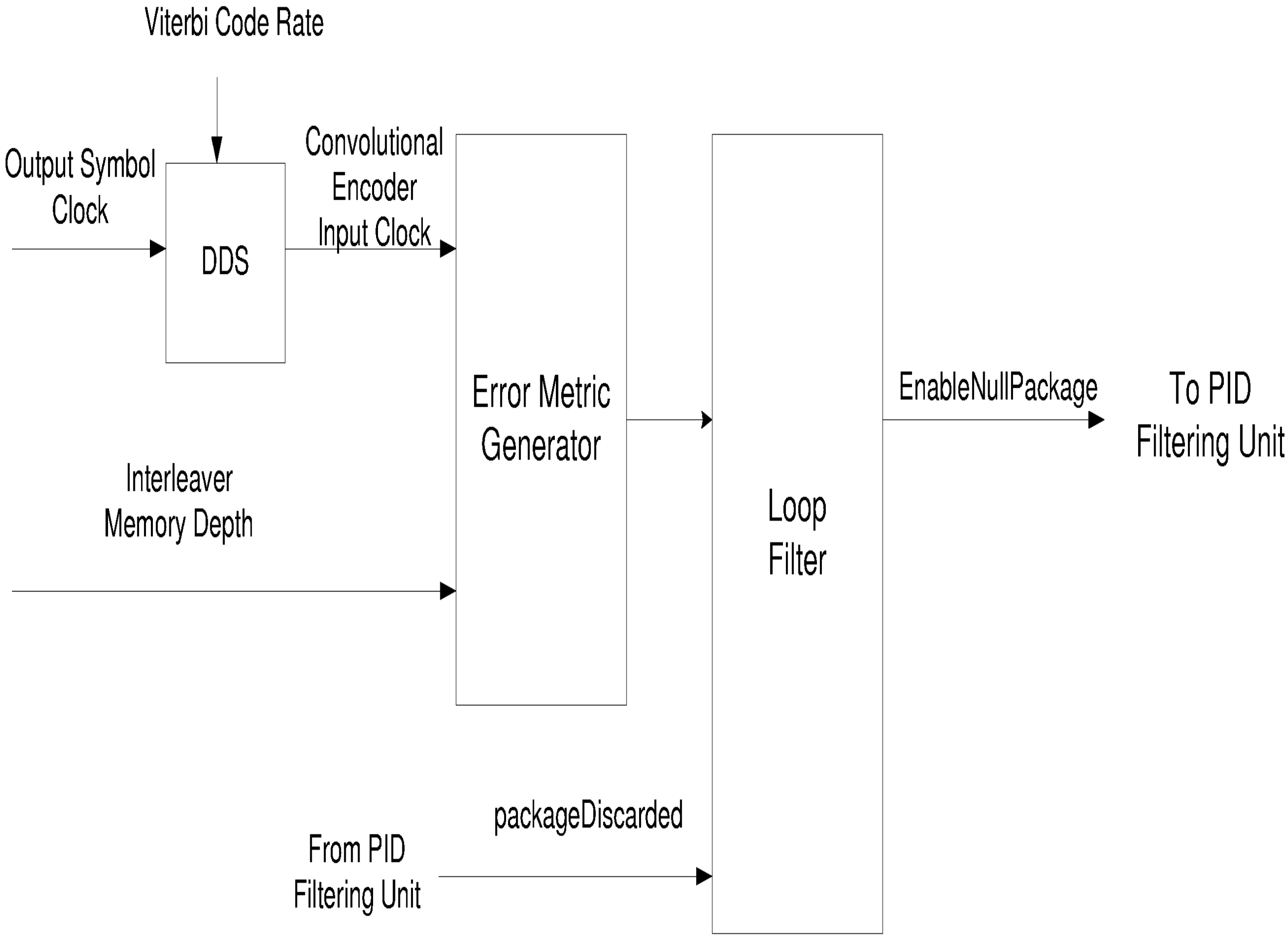

Figure 2.2: Possible Implementation of Rate Matching Unit.

2.3 PRC Restamping Unit

PRC Restamping can be performed or bypassed. However, it would be better to implement as a safe guard. It uses the input PRC time stamp to re-generate 27MHz clock. Then, re-stamp PRC stamp at the output of Rate Matching Unit.

As shown in Figure 2.3, the recovery of 27 MHz system clock consists of a timing recovery loop and a DDS. Because our design uses Interleaver buffer to de-jitter, the output of Rate Macthing Unit should keep a byte counter to emulate a constant bit rate output. The complexity of this circuitry is roughly equivalent to a BTL, a 30-bit DDS, a small state machine, and some simple logic.

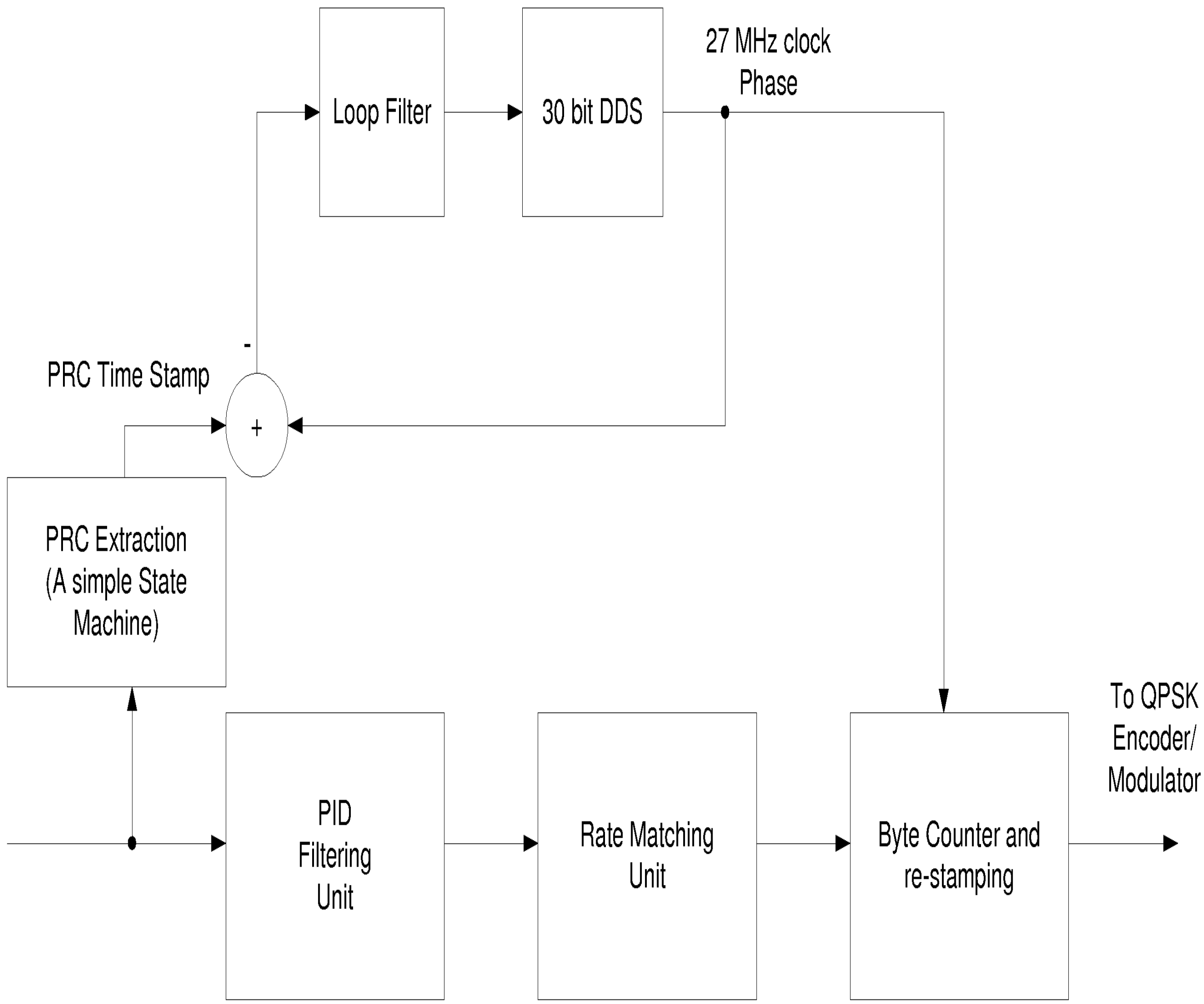

Figure 2.3: Possible Implementaion of PRC Re-stamping UNit.

3. QPSK Encoder and Modulator

The complexity of QPSK Encoder/Modulator is a straightforward implementation of DVB spec. It has been estimated to be 0.6 mm squared by Haifa team.

Mats mentioned that it would be simplify RF design if a digital filter that emphasizes the 3rd order harmonics can be included. This is still under investigation.

We will update this section later.

4. 13V/17V Slave Device

EchoStar Legacy mode uses the switching between 13V and 17V to transmit the message. Each bit interval is 8 ms. The slave device needs to synchronize the bit-boundary and detect the DC level. A 1-bit A2D similar to DiSeqC 2.1 receiver can be used. This is based on the assumption that generating a sampling clock just for this 1-bit A2D is wasting effort. The rest of the detection mechanism is similar to DiSEqC receiver.

It seems that very little extra gate counts are needed if a DiSEqC 1.0 slave device is included in Transcoder. However, it may increase the footprint of software due to protocol stack.

Questions to Marketing

1. *In order to perform channel change with EchoStar Legacy Mode, we need a protocol spec from EchoStar. Would they be able to release it?*
2. *Do we need DiSEqC 1.0 Slave Device? However, the implementation of DiSEqC 2.0 slave device will cost more and is not recommended.*

5. Complexity

Unit	Complexity
PID Filtering Unit in MPEG Remux	A state machine tracking PID position. A 13x32 memory for storing desired PID A 13-bit comparison logic. A 70-bit buffer.
Rate Matching Unit	The complexity is roughly the same as Clock Smooth Circuitry in Camaric.
PRC Re-stamping Unit	Same as BTL Camaric 30-bit DDS Small state machine a few logic
QPSK Encoder/ Modulator	0.6 mm sqrt per Haifa's estimation
13/17 V Slave Device	Similar to DiSeqC Receiver design in Camaric
Upper Converter	not covered in this memo
Micro-controller	Not covered in this memo